



Abstract

The cylindrical copper rollers are an essential part of the printing process. The copper roller needs to be finely finished to ensure the even distribution of the colors. Fine and precise polishing of cylindrical copper rollers is challenging using conventional finishing procedures because of their ductility and low hardness. Therefore, the magnetorheological finishing process based on three revolving flat-tip tools has been used to meet this precise requirement. The optimized parameters were found as current 3.54 for the electromagnet, rotating speed of the workpiece 510 rpm, revolving speed of the tools 35 rpm, working gap 0.7 mm and feed rate 150 mm/min for maximum percentage reduction in the surface roughness of copper roller. After 4 h of finishing with the optimal parametric settings, the Ra, Rq, and Rz values were reduced to 0.08. 0.1. and 0.67 µm from the initial values of 0.375. 0.527. and 1.96 µm. respectively. across the copper



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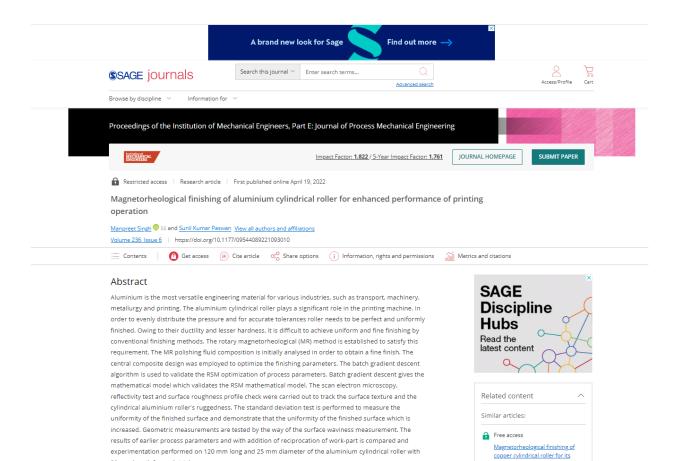






30 mm length for each trial.

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Original Paper | Published: 03 January 2021

CNTFET Based 4-Trit Hybrid Ternary Adder-Subtractor for low Power & High-Speed Applications

<u>Suman Rani</u> & <u>Balwinder Singh</u> □

<u>Silicon</u> **14**, 689–702 (2022) | <u>Cite this article</u>

138 Accesses | 7 Citations | Metrics

Abstract

To go through the phenomenon at nanoscale regimes, circuits using the CNTFETbased on Ternary Logic have been explored due to their constantly increasing application in high-speed low power designs. In this paper, 4-Trit Ternary Adder-Subtractor (TAS) using Complementary metal-oxide-semiconductor (CMOS) and Carbon Nanotube Field-Effect Transistor (CNFET) is proposed, which demonstrates the ternary addition and subtraction with a single circuit. The design style is based on conventional static CMOS implementation. The Fundamental ternary logic units are connected to achieve the required design. Therefore, prominence is given to the optimization of these fundamental units. The implementation and simulation are analyzed and validated using Hailey Simulation Program with Integrated

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Regular Paper | Published: 15 February 2021

CNTFET Based Ternary 1-Trit & 2-Trit Comparators for Low Power High-Performance Applications

Suman Rani, Balwinder Singh [™] & Rekha Devi

<u>Transactions on Electrical and Electronic Materials</u> 22, 734–749 (2021) <u>Cite this article</u>

97 Accesses | 2 Citations | Metrics

Abstract

1-Trit and 2-Trit Ternary comparator circuits using Complementary Metal—Oxide—Semiconductor (CMOS) as well as Carbon Nanotube Field-Effect Transistor (CNTFET) is proposed and investigated for Low Power High-performance applications. The design and simulation are investigated and authenticated using Hailey Simulation Program with Integrated Circuit (HSPICE) with Predictive technology model (PTM) low power 32 nm metal gate/High-K/Strained-Si Model for CMOS and 32 nm Stanford Model for CNTFET. The CNTFET based design is compared with the CMOS design in terms of significant design aspects, specifically delay, Average Power consumption and Power delay product (PDP). A comparison is performed among CMOS and CNTFET based ternary comparator circuits which reveals that CNTFETs can lead to more efficient ternary circuits. In terms of delay and power







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Home > Designs, Codes and Cryptography > Article

Published: 02 August 2019

Construction of girth-8 (3,L)-QC-LDPC codes of smallest CPM size using column multipliers

<u>Jasvinder Singh</u>, <u>Manish Gupta</u> $^{ extstyle \square}$ & <u>Jaskarn Singh Bhullar</u>

Designs, Codes and Cryptography 88, 41–49 (2020) Cite this article

229 Accesses | 2 Citations | Metrics

Abstract

In this paper, a new method for the construction of the exponent matrix of quasi-cyclic low-density parity-check (QC-LDPC) codes is proposed. The entries of the exponent matrix are based on the column multipliers. To find the column multipliers, a parameter S_{α} is defined which gives the value of column multiplier of the α th column. The proposed method reduced the complexity related to the formation of the exponent matrix and results in (3,L)-QC-LDPC codes with girth at least eight, for L>3. Also, a lower bound on the size of the circulant permutation matrix (CPM) for a QC-LDPC code is derived, and the codes constructed by this method are optimal to the given bound. Further, most of the codes constructed using this

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Journal of Green Engineering (JGE)

Volume-10, Issue-11, November 2020

Review of Application Industrial Robots

¹H S Gill and ²Arshdeep Singh Kalsi

¹Professor, Department of Mechatronics Engineering, Chandigarh University, Mohali, Punjab, India.

²Asst. Prof., Department of Mechanical Engineering, Baba Farid College of Engineering & Technology, Bathinda, India.

Abstract

Robotics is currently within an infantile period of invention which crosses engineering restrictions which are standard. The data their app demand knowledge of mechanical engineering, technology and technology and mathematics and the matter of robots. New technology areas, including technology has been recognized to handle the intricacy of factory automation and the robotics. This paper will reveal quite a few of those arms on the ground and will exhibit the parts of the arm and also the mechanisms. A number of the sections will reveal the classification of robotics generally to gain understanding of robotics, like classes, method and program location of control. Design issues go to be shown as the total amount of connectivity level, redundancy along with mobility. The traits of this hybrid arm's structure and also there is a demand while inside the use of buildings are reviewed. Vital phrases Serial manipulators, Hybrid arm manipulators

1 Introduction

Discovered plenty of experiments completed inside age and this afternoon because of hastened requirements using the arm on arm. The arm includes many edges which will possibly be far much greater when compared with



Published: 27 November 2019

On the search of smallest QC-LDPC code with girth six and eight

<u>Jasvinder Singh, Manish Gupta</u> ≥ <u>8 Jaskarn Singh Bhullar</u>

<u>Cryptography and Communications</u> **12**, 711–723 (2020) Cite this article

192 Accesses Metrics

Abstract

In this paper, a new and simple method for the construction of Girth-6 (J,L) Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) codes is proposed. The method is further extended to the search of Girth-8 QC-LDPC codes with base matrices of order $3 \times L$ and $4 \times L$. The construction is based on three different forms of exponent matrices and the parameters α , p, and q which satisfy the necessary algebraic conditions for a QC-LDPC code having girth 6 and 8. The proposed (J,L) QC-LDPC codes with girth at least six have optimal circulant permutation matrix (CPM) size for the cases where $q = \alpha + 1$. Moreover, most of the girth-8 QC-LDPC codes searched by the proposed method have smaller CPM size than the existing codes of the same girth. In several cases, the method gives more than one exponent matrices for a code, as most of the existing methods cannot do so. Besides this, the proposed method not only search the QC-LDPC codes with smaller CPM size but also takes much less time than the existing search based methods to search code.





Home > Journal of Electronic Materials > Article

Published: 25 February 2019

Parameterized Comparison of Nanotransistors Based on CNT and GNR Materials: Effect of Variation in Gate Oxide Thickness and Dielectric Constant

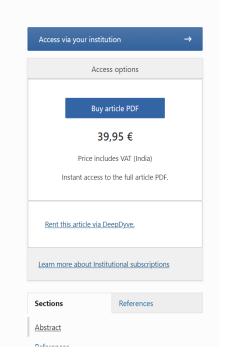
<u>Anjana Kumari, Suman Rani</u> & <u>Balwinder Singh</u> ⊡

Journal of Electronic Materials 48, 3078–3085 (2019) | Cite this article

183 Accesses 8 Citations Metrics

Abstract

Silicon based technology encounters scaling parameters that prohibit the advancement of transistor technology. Graphene nanoribbons (GNR) and carbon nanotubes (CNT) are often considered the predominating devices to replace silicon technology. Carbon nanotube field effect transistors (CNTFETs) are considered the most promising devices because of their most interesting properties such as high current carrying ability (\sim 1010 A/cm²), excellent carrier mobility, scalability, high reliability for elevated temperature operation, and negligible leakage current. In this paper, a comparative analysis of CNTFET and graphene nanoribbon field effect transistors (GNRFET) is presented. The results of simulations are presented, and comparisons of devices are done based on different parameters listed as $I_{\rm ON}/I_{\rm OFF}$ current



Journal of Nanoscience Nanoengineering and Applications

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HOME ABOUT LOGIN REGISTER SEARCH CURRENT ARCHIVES EDITORIAL BOARD STM HOME PAGE Home > Vol 8, No 2 (2018) > Rani	CURRENT ISSUE
in Open Access in Subscription or Fee Access Ternary Logic Design Approach - From CMOS to CNTFET Suman Rani, Gagandeep Kaur, Balwinder Singh Lakha Abstract	JONSNEA Menu JONSNEA Scope Call for Pager JONSNEA Indexing OPEN JOURNAL SYSTEMS Journal Helo
The goal of this review is to offer a broad study on the ternary logic designs based on CMOS (complementary metal-oxide-semiconductor) and CNTFET (carbon nanotube field effect transistor) suitable for energy efficient and high-performance VLSI design. Performance investigation of the ternary logic-based designs will be the primary emphasis as the ternary logic is a good substitute for the conventional binary logic among all the multiple-valued logics because it permits simple and power efficient digital design owing to the lessen chip area and circuit overhead due to interconnects. The usefulness of this paper lies in the field of academic and research related to low power and high-speed VLSI design, and nano-scale devices. A brief summary of ternary logic designs based on CMOS and CNTFET is presented. This study enables the reader to clear basic concepts about the ternary logic designs and their performance analysis. Keywords: CMOS, carbon nanotube field effect transistor (CNTFET), multi-valued logic (MVL) design, ternary logic, HSPICE	SUBSCRIPTION Login to verify subscription USER Username Password Remember me
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Ray HB, Anvar AZ, and Walt ADH. Carbon Nanotubes-the route toward applications. Science. 2002; 297(5582): 787-792 p. International Technology Roadmap for Semiconductors (ITRS), Emerging Research Device Summary, 2015 Singh A, Khosla M, Raj B. Comparative Analysis of Carbon Nanotube Field Effect Transistors.Proc. of GCCE; 2015 Chowdhury AH, Akhter N, and Faisal AA. Performance Analysis and Development of Self- Consistent Model of Carbon Nanotube Field Effect Transistor (CNTFET).	JOURNAL CONTENT Search Search Scope All Search
Proc. of the Global Engg, Sci. and Tech. conf.; 2012: 28-29p Moalyeri MH, Mirzaee RF, Navi. K et al. Efficient CNTFET-based Ternary Full Adder Cells for Nano-electronics, Nano-Micro Lett. 2011; 3(1): 43-50p. McEuen PL, Fuhrer M and Park H. Single-walled carbon nanotube electronics. IEEE Trans. on Nanotech. 2002; 99(1): 78-85p. Mukaidono M. Regular ternary logic functions—Ternary logic functions suitable for treating ambiguity. IEEE Trans. Comp.1982; C-35(2): 179-183p.	Browse By Issue By Author By Title Other Journals



<u>Home</u> > <u>Journal of Thermal Spray Technology</u> > Article

Peer Reviewed | Published: 17 August 2018

Enhancing Biocompatibility and Corrosion Resistance of Ti-6Al-4V Alloy by Surface Modification Route

Journal of Thermal Spray Technology 27, 1388–1400 (2018) | Cite this article

937 Accesses | 30 Citations | Metrics

Abstract

Titanium (Ti) and its alloys are widely used as candidate materials for biomedical implants. Despite their good biocompatibility and corrosion resistance, these materials suffer from corrosion after implantation in biological environments. The aim of this research work is to study the effect of two coatings on biocompatibility and corrosion behavior of Ti-6Al-4V biomedical implant material. Hydroxyapatite (HA) and hydroxyapatite/titanium dioxide (HA/TiO $_2$) coatings were thermal-sprayed on Ti-6Al-4V substrates. In the latter case, TiO $_2$ was used as a bond coat between the substrate and HA top coat. The corrosion behavior of coated and un-coated samples in Ringer's solution was studied by potentiodynamic and linear polarization techniques. Before and after corrosion testing, XRD and SEM/EDS techniques were used for the analysis of phases formed and to investigate microstructure/compositional changes in the coated specimens. The cellular response was analyzed by the MTT



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Figures Refere



Home / Journal of Nanoelectronics and Optoelectronics, Volume 13, Number 1



Investigation of Schottky Barrier, Conventional and Tunnel Carbon Nanotube Field Effect Transistor for Low Power Design

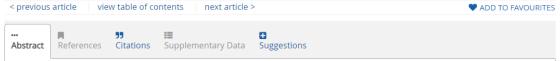


Authors: Rani, Suman; Singh, Balwinder

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Publisher: American Scientific Publishers **DOI:** https://doi.org/10.1166/jno.2018.2169





In past few years, the Field-effect transistor based on Semiconducting Carbon Nanotube (CNT) have generated the consideration for low power device due to its quasi-ideal electronics properties and high-level performance. In this paper, a comparative study of Schottky Barrier, Conventional and Tunnel Carbon Nanotube Field Effect Transistor (CNTFET) is presented based on operation, characteristics and structure. These three devices are simulated using Nano TCAD VIDES for double gate planar geometry and 3-Dimensional structures. The results are presented based on the performance parameters like On current ($I_{\rm ON}$), Off current ($I_{\rm OF}$) and the ratio of On current to Off current ($I_{\rm ON}$), $I_{\rm OFF}$). Effective Performance is analyzed with variation in Drain to source voltage $I_{\rm OF}$, Channel length ($I_{\rm OF}$), Diameter ($I_{\rm ON}$) and thickness Oxide ($I_{\rm OX}$) keeping other parameters constant. From the simulated results it has been observed that Tunnel Carbon Nanotube Field Effect Transistor (T-CNFET) delivers the best performance as compared to Conventional, Schottky Barrier i.e., maximum $I_{\rm ON}$ ($I_{\rm OFF}$) = 6.88E + 08 at $I_{\rm OS}$ = 0.1 V, $I_{\rm OF}$ = 20 nm, $I_{\rm OS}$ = 1 nm and $I_{\rm OS}$ = 1 nm.

Keywords: CARBON NANOTUBE; CONVENTIONAL CNTFET; NANO TCAD VIDES; SCHOTTKY BARRIER CNTFET; TUNNEL CNTFET

Document Type: Research Article



